IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A logic circuit for generating four binary outputs as four threshold functions of four binary inputs to the logic circuit, the threshold functions comprising a first threshold function which is high if at least one of the binary inputs is high, a second threshold function which is high if at least two of the binary inputs are high, a third threshold function which is high if at least three of the binary inputs are high, and a fourth threshold function which is high if all of the binary inputs are high, the logic circuit comprising:

first level logic comprising two logic parts, each logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving the binary inputs and two first level outputs; and

second level logic comprising four second level outputs, four second level inputs for receiving second level binary inputs and connected to the four first level outputs, a NAND gate, a first gate generating a logical OR combination of two second level binary inputs and NAND combining the logical OR combination with two other second level binary inputs, a second gate generating logical OR combinations of two pairs of second level binary inputs and NAND combining the logical OR combinations, and a NOR gate;

wherein one of said four binary outputs is generated at each of said four outputs.

2. (Currently Amended) A logic circuit according to claim 1, wherein said first gate comprises ~~an AOI211 gate~~ an $((A+B)CD)^c$ gate to implement the logic equation $((A+B)CD)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $((A+B)CD)^c$ gate.

3. (Currently Amended) A logic circuit according to claim 1, wherein said second gate comprises ~~an OAI22 gate~~ an $((A+B)(C+D))^c$ gate to implement the logic equation $((A+B)(C+D))^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes

complement, and A, B, C, D denote inputs to said $((A+B)(C+D))^c$ gate.

4. (Original) A parallel counter including the logic circuit according to claim 1.

5. (Original) A logic circuit for generating four binary outputs as four threshold functions of four binary inputs to the logic circuit, the threshold functions comprising a first threshold function which is high if at least one of the binary inputs is high, a second threshold function which is high if at least two of the binary inputs are high, a third threshold function which is high if at least three of the binary inputs are high, and a fourth threshold function which is high if all of the binary inputs are high, the logic circuit comprising:

first level logic comprising two logic parts, each logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving the binary inputs and two first level outputs; and

second level logic comprising four second level outputs, four second level inputs for receiving second level binary inputs and connected to the four first level outputs, a NAND gate, a first gate generating logical AND combinations of two pairs of second level binary inputs and NOR combining the logical AND combinations, a second gate generating logical OR combinations of two pairs of second level binary inputs and NAND combining the logical OR combinations, and a NOR gate;

wherein one of said four binary outputs is generated at each of said four outputs.

6. (Currently Amended) A logic circuit according to claim 5, wherein said first gate comprises ~~an AOI22 gate~~ an $(AB+CD)^c$ gate to implement the logic equation $(AB+CD)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $(AB+CD)^c$ gate.

7. (Currently Amended) A logic circuit according to claim 5, wherein said second gate comprises ~~an OAI22 gate~~ an $((A+B)(C+D))^c$ gate to implement the logic equation $((A+B)(C+D))^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes

complement, and A, B, C, D denote inputs to said $((A+B)(C+D))^c$ gate.

8. (Original) A parallel counter including the logic circuit according to claim 5.

9. (Original) A logic circuit for generating three binary outputs as three threshold functions of binary inputs to the logic circuit, the threshold functions comprising a first threshold function which is high if at least one of the binary inputs is high, a second threshold function which is high if at least two of the binary inputs are high, and a third threshold function which is high if all of the binary inputs are high, the logic circuit comprising:

first level logic comprising two logic parts, a first logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving two of the binary inputs and two first level outputs, and a second logic part comprising an inverter having one first level logic input for receiving one of the binary inputs and one first level output; and

second level logic comprising three second level outputs, and three second level inputs for receiving second level binary inputs and connected to the three first level outputs, a NAND gate, a gate generating a logical AND combination of two second level binary inputs and NOR combining the logical AND combination with one other second level binary input, and a NOR gate;

wherein one of said three binary outputs is generated at each of said three outputs.

10. (Currently Amended) A logic circuit according to claim 9, wherein said first gate comprises ~~an AOI21 gate~~ an $(AB+C)^c$ gate to implement the logic equation $(AB+C)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C denote inputs to said $(AB+C)^c$ gate.

11. (Original) A parallel counter including the logic circuit according to claim 9.

12. (Original) A logic circuit for generating three binary outputs as three threshold functions of binary inputs to the logic circuit, the threshold functions comprising a first threshold function

which is high if at least one of the binary inputs is high, a second threshold function which is high if at least two of the binary inputs are high, and a third threshold function which is high if all of the binary inputs are high, the logic circuit comprising:

first level logic comprising two logic parts, a first logic part comprising a NOR gate and a NAND gate and having two first level inputs for receiving two of the binary inputs and two first level outputs, and a second logic part comprising an inverter having one first level logic input for receiving one of the binary inputs and one first level output; and

second level logic comprising three second level outputs, and three second level inputs for receiving second level binary inputs and connected to the three first level outputs, a NAND gate, a gate generating a logical OR combination of two second level binary inputs and NAND combining the logical OR combination with one other second level binary input, and a NOR gate;

wherein one of said three binary outputs is generated at each of said three outputs.

13. (Currently Amended) A logic circuit according to claim 12, wherein said first gate comprises ~~an OAI21 gate~~ an $((A+B)C)^c$ gate to implement the logic equation $((A+B)C)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C denote inputs to said $((A+B)C)^c$ gate.

14. (Original) A parallel counter including the logic circuit according to claim 12.

15. (Original) A logic circuit having seven binary inputs, the logic circuit comprising:

first logic for generating a first binary value as a threshold function which is high if at least four binary inputs are high, a second binary value as a threshold function which is high if less than two binary inputs are high, and a third binary value as a threshold function which is high if less than six binary inputs are high; and

second logic for forming the OR combination of the first binary value and the second binary value and for NAND combining the third binary value and the result of the OR combination.

16. (Original) A logic circuit according to claim 15, wherein said second logic comprises an inverting gate.

17. (Currently Amended) A logic circuit according to claim 15, wherein said second logic comprises ~~an OA121 gate~~ an $((A+B)C)^c$ gate to implement the logic equation $((A+B)C)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C denote inputs to said $((A+B)C)^c$ gate.

18. (Original) A logic circuit according to claim 15, wherein said first binary logic comprises four first logic parts having four of the binary inputs for generating a fourth binary value as a threshold function which is high if at least one of the four binary inputs is high, a fifth binary value as a threshold function which is high if at least two of the four binary inputs are high, a sixth binary value as a threshold function which is high if at least three of the four binary inputs are high, and a seventh binary value as a threshold function which is high if all of the four binary inputs are high; three second logic parts having three of the binary inputs for generating an eighth binary value as a threshold function which is high if at least one of the three binary inputs is high, a ninth binary value as a threshold function which is high if at least two of the three binary inputs are high, and a tenth binary value as a threshold function which is high if all of the three binary inputs are high; first combining logic for combining said fourth binary value, said fifth binary value, said eighth binary value, and said ninth binary value to generate said second binary value; and second combining logic for combining said sixth binary value, said seventh binary value, said ninth binary value, and said tenth binary value to generate said third binary value.

19. (Original) A logic circuit according to claim 18, wherein said first combining logic comprises logic for logically AND combining said fourth binary value and said eighth binary value, and for logically NOR combining said fifth binary value, said ninth binary value, and the results of the logical combination.

20. (Original) A logic circuit according to claim 19, wherein said first combining logic comprises an inverting gate.

21. (Currently Amended) A logic circuit according to claim 19, wherein said first combining logic comprises ~~an AOI211 gate~~ an $(AB+C+D)^c$ gate to implement the logic equation $(AB+C+D)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $(AB+C+D)^c$ gate.

22. (Original) A logic circuit according to claim 18, wherein said first combining logic comprises logic for logically OR combining said fifth binary value and said eighth binary value, and for logically OR combining said fourth binary value, said ninth binary value, and for logically NAND combining the results of the logical combinations.

23. (Original) A logic circuit according to claim 22, wherein said first combining logic comprises an inverting gate.

24. (Currently Amended) A logic circuit according to claim 22, wherein said first combining logic comprises ~~an AOI22 gate~~ an $((A+B)(C+D))^c$ gate to implement the logic equation $((A+B)(C+D))^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $((A+B)(C+D))^c$ gate.

25. (Original) A logic circuit according to claim 18, wherein said second combining logic comprises logic for logically AND combining said sixth binary value and said tenth binary value, for logically AND combining said seventh binary value and said ninth binary value, and for logically NOR combining the results of the logical combinations.

26. (Original) A logic circuit according to claim 25, wherein said second combining logic comprises an inverting gate.

27. (Currently Amended) A logic circuit according to claim 25, wherein said second combining logic comprises ~~an AOI22 gate~~ an $(AB+CD)^c$ gate to implement the logic equation $(AB+CD)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $(AB+CD)^c$ gate.

28. (Original) A logic circuit according to claim 19, wherein said second combining logic comprises logic for logically AND combining said sixth binary value and said tenth binary value, for logically AND combining said seventh binary value and said ninth binary value, and for logically NOR combining the results of the logical combinations.

29. (Original) A logic circuit according to claim 28, wherein said second combining logic comprises an inverting gate.

30. (Currently Amended) A logic circuit according to claim 28, wherein said second combining logic comprises ~~an AOI22 gate~~ an $((A+B)(C+D))^c$ gate to implement the logic equation $((A+B)(C+D))^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $((A+B)(C+D))^c$ gate.

31. (Original) A logic circuit according to claim 22, wherein said second combining logic comprises logic for logically AND combining said sixth binary value and said tenth binary value, for logically AND combining said seventh binary value and said ninth binary value, and for logically NOR combining the results of the logical combinations.

32. (Original) A logic circuit according to claim 31, wherein said second combining logic comprises an inverting gate.

33. (Currently Amended) A logic circuit according to claim 31, wherein said second combining logic comprises ~~an AOI22 gate~~ an $(AB+CD)^c$ gate to implement the logic equation $(AB+CD)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes

complement, and A, B, C, D denote inputs to said $(AB+CD)^c$ gate.

34. (Original) A logic circuit having seven binary inputs, the logic circuit comprising:

first logic for generating a first binary value as a threshold function which is high if at least four binary inputs are high, a second binary value as a threshold function which is high if less than two binary inputs are high, and a third binary value as a threshold function which is high if less than six binary inputs are high; and

an inverting multiplexer to select and output the inverse of the second or third binary value dependant upon the first binary value.

35. (Original) A logic circuit according to claim 34, wherein said first binary logic comprises four first logic parts having four of the binary inputs for generating a fourth binary value as a threshold function which is high if at least one of the four binary inputs is high, a fifth binary value as a threshold function which is high if at least two of the four binary inputs are high, a sixth binary value as a threshold function which is high if at least three of the four binary inputs are high, and a seventh binary value as a threshold function which is high if all of the four binary inputs are high; three second logic parts having three of the binary inputs for generating an eighth binary value as a threshold function which is high if at least one of the three binary inputs is high, a ninth binary value as a threshold function which is high if at least two of the three binary inputs are high, and a tenth binary value as a threshold function which is high if all of the three binary inputs are high; first combining logic for combining said fourth binary value, said fifth binary value, said eighth binary value, and said ninth binary value to generate said second binary value; and second combining logic for combining said sixth binary value, said seventh binary value, said ninth binary value, and said tenth binary value to generate said third binary value.

36. (Original) A logic circuit according to claim 35, wherein said first combining logic comprises logic for logically AND combining said fourth binary value and said eighth binary value, and for logically NOR combining said fifth binary value, said ninth binary value, and the results of the logical combination.

37. (Original) A logic circuit according to claim 35, wherein said first combining logic comprises an inverting gate.

38. (Currently Amended) A logic circuit according to claim 35, wherein said first combining logic comprises ~~an AOI211 gate~~ an $(AB+C+D)^c$ gate to implement the logic equation $(AB+C+D)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $(AB+C+D)^c$ gate.

39. (Original) A logic circuit according to claim 35, wherein said first combining logic comprises logic for logically OR combining said fifth binary value and said eighth binary value, and for logically OR combining said fourth binary value, said ninth binary value, and for logically NAND combining the results of the logical combinations.

40. (Original) A logic circuit according to claim 35, wherein said first combining logic comprises an inverting gate.

41. (Currently Amended) A logic circuit according to claim 35, wherein said first combining logic comprises ~~an OAI22 gate~~ an $((A+B)(C+D))^c$ gate to implement the logic equation $((A+B)(C+D))^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $((A+B)(C+D))^c$ gate.

42. (Original) A logic circuit according to claim 35, wherein said second combining logic comprises logic for logically AND combining said sixth binary value and said tenth binary value, for logically AND combining said seventh binary value and said ninth binary value, and for logically NOR combining the results of the logical combinations.

43. (Original) A logic circuit according to claim 42, wherein said second combining logic comprises an inverting gate.

44. (Currently Amended) A logic circuit according to claim 42, wherein said second combining logic comprises ~~an AOI22 gate~~ an $(AB+CD)^c$ gate to implement the logic equation $(AB+CD)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $(AB+CD)^c$ gate.

45. (Original) A logic circuit according to claim 36, wherein said second combining logic comprises logic for logically AND combining said sixth binary value and said tenth binary value, for logically AND combining said seventh binary value and said ninth binary value, and for logically NOR combining the results of the logical combinations.

46. (Original) A logic circuit according to claim 45, wherein said second combining logic comprises an inverting gate.

47. (Currently Amended) A logic circuit according to claim 45, wherein said second combining logic comprises ~~an AOI22 gate~~ an $(AB+CD)^c$ gate to implement the logic equation $(AB+CD)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes complement, and A, B, C, D denote inputs to said $(AB+CD)^c$ gate.

48. (Original) A logic circuit according to claim 39, wherein said second combining logic comprises logic for logically AND combining said sixth binary value and said tenth binary value, for logically AND combining said seventh binary value and said ninth binary value, and for logically NOR combining the results of the logical combinations.

49. (Original) A logic circuit according to claim 48, wherein said second combining logic comprises an inverting gate.

50. (Currently Amended) A logic circuit according to claim 48, wherein said second combining logic comprises ~~an AOI22 gate~~ an $(AB+CD)^c$ gate to implement the logic equation $(AB+CD)^c$, wherein + denotes logical OR, proximity denotes logical AND, ^{c} denotes

complement, and A, B, C, D denote inputs to said $(AB+CD)^c$ gate.

51. (Original) A parallel counter including the logic circuit according to claim 15.

52. (Original) A parallel counter including the logic circuit according to claim 34.